REMARKS

This Amendment responds to the Office Action dated April 15, 2004 in which the Examiner objected to the drawings and rejected claims 1-6 under 35 U.S.C. §103.

As indicated above, the specification has been amended to clearly refer to reference numeral 26 found in Figure 1. Support for this amendment can be found on page 8 line 20 and page 9 lines 5-6 of the specification. Applicants respectfully submit that no new matter has been added. Therefore, Applicants respectfully request the Examiner withdraws the objection to the drawings.

As indicated above, the typographical error in claim 4 has been corrected. Applicants respectfully request the Examiner approves the correction. Applicants furthermore respectfully submit that the amendment to claim 4 is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claim 1 claims a scan test system for a semiconductor device comprising first and second semiconductor devices and an analog wiring. The first semiconductor device includes a first analog input/output pin existing on the analog input side thereof, a first internal circuit, and a scan register connected between the first input/output pin and the first internal circuit. The second semiconductor device includes a second analog input/output pin on the analog input side thereof, a second internal circuit, and a scan register connected between the second input/output pin and the second internal circuit. The analog wiring connects the first analog input/output pin and the second analog input/output pin.

Through the structure of the claimed invention having a) a first semiconductor device including a first analog input/output pin, a first internal circuit and a scan register connected therebetween, b) a second semiconductor device including a second analog input/output pin, a second internal circuit and a scan register connected therebetween and c) analog wiring as claimed in claim 1, the claimed invention provides a scan test system in which a short/opening of a wiring analog-connected between devices can be inspected without probe inspection. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 4 claims a scan test system for a semiconductor device comprising a semiconductor device including first and second scan registers, first and second registers chains and a switching means. The first scan register is connected between a digital/analog double function pin on the input side and an internal circuit. The second scan register is connected between a digital input/output pin and the internal circuit. The first register chain serially connects a plurality of the first scan registers, each fetching the data input and outputting the result to the output side. The second register chain is connected to the first register chain and simultaneously serially connects a plurality of the second scan registers, each fetching the data input and outputting the result to the output side. The switching means bypasses at least one of the first and the second register chains and thereby connects the data input to the output side.

Through the structure of the claimed invention having a) a first scan register connected between a digital-analog double function pin and an internal circuit, b) a second scan register connected between a digital input/output pin and the internal circuit, c) first and second register chains and d) a switching means bypassing at

least one of the first and second register chains as claimed in claim 4, the claimed invention provides a scan test system which can carry out bulk inspection using a double-functional pin with another dedicated digital pin to improve inspection efficiency. The prior art does not show, teach or suggest the invention as claimed in claim 4.

Claims 1-2 were rejected under 35 U.S.C. §103 as being unpatentable over *Russell* (U.S. Patent No. 5,404,358) in view of *Tsukimori et al.* (U.S. Patent No. 6,708,304).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Russell appears to disclose FIG. 1 shows standard test access port (TAP) which implements boundary scan testing altered to incorporate the analog test circuits. A substantial portion of the circuits in FIG. 1 included in a digital control section such as block 150 corresponds to the circuits. The circuits of FIG. 1 provide two modes of operation: analog and digital. In the analog mode, analog signals or levels may be transmitted between circuitry external to an IC device and analog circuitry within the IC or to other ICs containing the interface circuits. The analog circuits include analog switches 126, 132, 128 and analog switch matrices 134, 136 and 138 connected as shown. Analog switches 126 and 132 provide isolation to prevent interference by digital circuitry of block 150 during analog measurements. (col. 4, lines 32-55) Analog switch 128 is used to pass analog signals bi-directionally between pins TDI and TDO during analog operations when other ICs are selecting

measurement points or when an analog switch matrix directly connected to one of the two pins TDI and TDO is required to be connected to the other pin. The analog switch matrices 134, 136 and 138 are groups of analog switches for connecting pins TDI and TDO, and internal IC device reference points to test and control points within the IC device, separately or together, as desired. In the preferred embodiment, each system functional input and output pin of the IC device (not shown) is connected to each of the three matrices 134, 136 and 138. (col. 5, line 13-30) Analog control decoder 124 drives the various analog switch control gate inputs G over the set of lines 130 according to the contents previously loaded into an analog control register 122, connected to decoder 124 via lines 123, output of an instruction decoder 108, connected to decoder 124 via lines 114, and the state of a test access port (TAP) controller 110, connected to decoder 124 via lines 112. In particular, the TAP controller Run-Test/Idle state is utilized. For clarity, lines 112 and lines 114 are combined as lines 113 in FIG. 1. In the preferred embodiment, signal TCK is among the signals applied to lines 112 and 113 to allow alternate matrix selection without having to alter the contents of analog control register 122. (col. 5, lines 47-60) In the standard boundary scan architecture, there are three digital shift registers in the TDI to TDO data path. These are instruction register 106, bypass register 102 and boundary scan register 100. The first register 106 provides a means for shifting and holding both standard and optional instructions transmitted over the TDI to TDO path from outside the IC. (col. 6, lines 6-12) An AND gate 144, multiplexer 118 and driver 120 complete the TDI to TDO path of section 150 of FIG. 1. Gate 144 which is optional, buffers the digital shift registers 100, 102, 106 and 122 from analog signals arriving at the TDI pin connection when optional switch 126 is omitted. Multiplexer

118 selects the digital register to be used in the TDI to TDO data path according to contents of the instruction register 106 and state of TAP controller 110 decoded by instruction decoder 108 and applied via lines 117. (col. 6, lines 26-35)

Thus, *Russell* merely discloses a digital control section 150 including a boundary scan register 100 connected between a AND gate 144 and a multiplexer 118. Nothing in *Russell* shows, teaches or suggests a) a first semiconductor device including a first analog input/output pin, a first internal circuit and a scan register connected therebetween, b) a second semiconductor device including a second analog input/output pin, a second internal circuit and a scan register connected therebetween and c) analog wiring connecting the first and second analog input/output pins as claimed in claim 1. Rather, *Russell* merely discloses a single boundary scan register 100 found within a digital control section 150 and connected between a AND gate 144 and a multiplexer 118.

Tsukimori et al. appears to disclose a semiconductor device comprising an internal circuit, a port circuit connected to the internal circuit, external terminals to which the port circuit is connected, and a boundary scanning circuit, wherein the boundary scanning circuit is the one that makes access to the external terminals through test access terminals, the test access terminals are also used as predetermined external terminals among the external terminals, selection means is provided for selectively determining whether the multi-use terminals be connected to the port circuit or to the boundary scanning circuit, the selection means selecting, as an initial state, the state where the multi-use terminals are connected to the boundary scanning circuit in response to the power-on reset. (col. 2, lines 24-37) FIG. 19 illustrates an example of the electronic circuit using the above

microcomputer 1. The electronic circuit includes the microcomputer 1 as well as other semiconductor devices 81 and 82 mounted on the wiring board 80. In the microcomputer 1 as described above, the test access terminals for the boundary scanning are also used as other port terminals. The other semiconductor devices 81 and 82, too, have the boundary scanning function and their test access terminals may be the dedicated ones or may be the multi-use terminals as described above. In short, the test access terminals may be the dedicated ones when there is a margin in the number of the external terminals owing to the package size of the semiconductor device or when no compatibility is required concerning the arrangement of pins relative to the semiconductor device of the same kind without the boundary scanning function. In FIG. 19, on the circuit board 80 are formed first wirings 85A and 85B to which are connected the multi-use terminals of the microcomputer 1, and a second wiring 86 to which are connected the external terminals except the multi-use terminals of the semiconductor device. The external terminals of the microcomputer 1 are arranged like an array on one surface of the package so as to be surface-mounted. Even when the external terminals are arranged in the form an array on the back surface of the package, the defective connection between the microcomputer 1 and the circuit board 80 can be easily verified by using the boundary scanning circuit. The first wiring 85A on the circuit board 80 is dedicated to the boundary scanning. When the boundary scanning function is used, therefore, the multi-use terminals P1 to P5 that are also used as test access terminals on the circuit board, are no longer utilizable for transmitting signals to the input/output port circuit. Therefore, the external terminals that are also used as the test access terminals are those external terminals that are assigned to inputting/outputting signals that are

judged to be used less frequently. The situation is quite the same even for the external terminals Pj to Pj+5 that are also used for connection to the debugging circuit. (col. 13, line 44 through col. 14, line 13)

Thus, *Tsukimori et al.* merely discloses a microcomputer 1 as well as other semiconductor devices 81 and 82 mounted on a wiring board 80 which can be verified using a boundary scan circuit. However, nothing in *Tsukimori et al.* shows, teaches or suggests the configuration of the boundary scan circuit. In particular, nothing in *Tsukimori et al.* shows, teaches or suggests a) a first semiconductor device including a first analog input/output pin, a first internal circuit and a scan register connected therebetween, b) a second semiconductor device including a second analog input/output pin, a second internal circuit and a scan register connected therebetween and c) analog wiring connecting the first and second analog input/output pins as claimed in claim 1. Rather, *Tsukimori et al.* merely discloses a circuit board 80 which can be verified using boundary scanning circuits.

Since nothing in *Russell* or *Tsukimori et al.* show, teach or suggest the invention as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claim 2 depends from claim 1 and recites additional features. Applicants respectfully submit that claim 2 would not have been obvious within the meaning of 35 U.S.C. §103 over *Russell* and *Tsukimori et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 2 under 35 U.S.C. §103.

Claim 3 was rejected under 35 U.S.C. §103 as being unpatentable over *Russell* and *Tsukimori et al.* further in view of *Blair et al.* (U.S. Patent No. 5,428,624).

Applicants respectfully traverse the Examiner's rejection of the claim under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in the primary references of *Russell* and *Tsukimori et al.* show, teach or suggest the primary features as claimed in claim 1, Applicants respectfully submit that the combination of the primary references with the secondary reference to *Blair et al.* will not overcome the deficiencies of the primary references. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 3 under 35 U.S.C. §103.

Claims 4 and 6 were rejected under 35 U.S.C. §103 as being unpatentable over *Russell* in view of *Sturges* (U.S. Patent No. 5,491,666) and *Bloker et al.* (U.S. Patent No. 5,768,196).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to claims and allows the claims to issue.

As discussed above, *Russell* merely discloses a boundary scan register 100 found within a digital control section 150 and connected between a AND gate 144 and a multiplexer 118. Nothing in *Russell* shows, teaches or suggests a) a first scan register connected between a digital/analog <u>double function pin</u> and an internal circuit, b) a second scan register connected between a digital input/output pin and the internal circuit, c) first and second register chains and d) a switching means as

claimed in claim 4. Rather, *Russell* merely discloses a single boundary scan register 100 connected between a AND gate 144 and a multiplexer 118.

Surges appears to disclose a block diagram illustrating an integrated circuit 22 which includes a boundary-scan test circuit arrangement. In general, the boundary-scan circuitry is the only portion of the integrated circuit 22 which is illustrated in detail in FIG. 2. As may be seen, the circuit 22 has four terminals through which signals are transferred to the boundary-scan circuitry. These are a test data in (TDI) terminal, a test data out (TDO) terminal, a test mode select (TMS) terminal, and a test clock (TCK) terminal. Within the circuit 22 are a number of individual boundary-scan cells 26. Each of the boundary-scan cells 26 is functionally one stage of a shift register within that particular integrated circuit. Each boundary-scan cell 26 may be positioned adjacent an external pin 27 on the particular integrated circuit. Data may be provided to or received from a boundary-scan cell 26 at the pin 27 through a buffer stage 28. Each boundary-scan cell 26 may also be connected to provide or accept data from core logic circuitry within the integrated circuit 22. (col. 4, lines 37-65) FIG. 3 illustrates a typical boundary-scan circuitry within circuit 22. (col. 5, lines 21-22) As may be seen, the instruction controls the operation of a multiplexor 41 which controls the data path taken through the particular portion of the boundary-scan circuitry. Control signals from the boundary-scan controller circuit 30 also control a second multiplexor 42 which selects data from the path through the instruction register 33 or the data registers 29, 32, 34, and 35. A gate 43 is enabled when the test function of the boundary-scan circuitry is enabled by the TMS signals to allow data to flow to the TDO terminal. Thus, as may be seen, a serial path is provided through the boundary-scan circuitry of the circuit 22. Data may be

transferred bit by bit through this serial path from the TDI terminal to the TDO terminal. (col. 5, line 61 through col. 6, line 6)

Thus, *Sturges* merely discloses in Figure 3 the structure of a boundary scan circuitry formed within a circuit 22. Nothing in *Sturges* shows, teaches or suggests a) a first scan register connected between a digital/analog double function pin and an internal circuit, b) a second scan register connected between a digital input/output pin and the internal circuit, c) first and second register chains and d) a switching means as claimed in claim 4. Rather, *Sturges* merely discloses the architecture of a typical boundary scan circuitry within a circuit 22.

Bloker et al. appears to disclose a first-in-first-out ("FIFO") memory having a shift register based row decoder and memory redundancy. (col. 1, lines 7-9) Another feature is to provide a FIFO memory having a shift register based row decoder and memory redundancy. A further feature is to provide a redundant structure suitable for FIFO memories. (col. 2, lines 1-5) Referring to FIG. 4, the circuits of row select circuit 36 and redundant row select circuit 37 are shown. As can be seen from FIG. 4, circuit 36 includes a number of shift registers 50 through 52n that are serially connected together via a number of switching elements (e.g., switching elements 50a-50b, 51a-51b, and 52a-52b). As can be seen from FIG. 4, each of shift registers 50-52n is connected to two switching elements, one at the input (i.e., the D input) of the shift register and the other at the output (i.e., Q output) of the shift register. In addition, each of shift registers 50-52n has a bypassing transistor connected in parallel with the corresponding shift register. (col. 4, lines 4-16)

Thus, *Bloker et al.* merely discloses a FIFO memory having a shift register based row decoder and memory redundancy and including shift registers connected between switching elements. In other words, nothing in *Bloker et al.* shows, teaches or suggests a scan test system. Therefore, *Bloker et al.* is not a proper reference. In particular, nothing in *Bloker et al.* shows, teaches or suggests a) first and second scan registers, b) first and second register chains and c) a switching means bypassing the first and second register chains as claimed in claim 4.

The combination of *Russell*, *Sturges* and Bloker would not be possible since *Bloker et al.* is not directed to a scan test system. Even assuming arguendo that the references could be combined, nothing in the combination of the references show, teach or suggest the features as claimed in claim 4. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 4 under 35 U.S.C. 103.

Claim 6 depends from claim 4 and recites additional features. Applicants respectfully submit that claim 6 would not have been obvious within the meaning of 35 U.S.C. §103 over *Russell*, *Sturges* and *Bloker et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 6 under 35 U.S.C. §103.

Claim 5 was rejected under 35 U.S.C. §103 as being unpatentable over *Russell*, *Sturges* and *Bloker et al.* and further in view of *Blair et al.*

Applicants respectfully traverse the Examiner's rejection of the claim under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in the primary references of *Russell*, *Sturges* and *Bloker et al.* show, teach or suggest the primary features as claimed in claim 4, Applicants respectfully submit that the combination of the primary references with the secondary reference to *Blair et al.* will not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 5 under 35 U.S.C. §103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the current set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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